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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b> <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>		Attorney Docket No. <b>MI22-1384</b>
		First Inventor or Application Identifier <b>Moore</b>
		Title <b>Methods of Forming Oxide Regions Over...</b>
		Express Mail Label No. <b>6240750402</b>

<b>APPLICATION ELEMENTS</b> <small>See MPEP chapter 600 concerning utility patent application contents.</small>		<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. <input checked="" type="checkbox"/> * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)	6. <input type="checkbox"/> Microfiche Computer Program (Appendix)		
2. <input checked="" type="checkbox"/> Specification [Total Pages <b>24</b> ] (preferred arrangement set forth below) - Descriptive title of the Invention (plus cover pg.) - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure	7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies		
3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets <b>4</b> ]			
4. Oath or Declaration [Total Pages <b>2</b> ] a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below] i. <input type="checkbox"/> <b>DELETION OF INVENTOR(S)</b> Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).			
5. <input type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.			
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<b>ACCOMPANYING APPLICATION PARTS</b>	
8. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s))	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICATION FOR LETTERS PATENT**

\* \* \* \* \*

**Methods of Forming Oxide Regions Over  
Semiconductor Substrates, and Methods of  
Forming Transistors Associated With  
Semiconductor Substrates**

\* \* \* \* \*

INVENTORS

John T. Moore

ATTORNEY'S DOCKET NO. MI22-1384

1       **Methods of Forming Oxide Regions Over Semiconductor Substrates,**  
2       **and Methods of Forming Transistors Associated With**  
3       **Semiconductor Substrates**

4       **TECHNICAL FIELD**

5       The invention pertains to methods of forming oxide regions over  
6       semiconductor substrates, and in particular embodiments pertains to  
7       methods of forming two or more transistors associated with a  
8       semiconductor substrate.

9  
10      **BACKGROUND OF THE INVENTION**

11      Oxide regions, such as, for example, silicon dioxide regions, have  
12      numerous applications in semiconductor devices. For instance, a thin  
13      layer of silicon dioxide is frequently placed between the conductive  
14      material of a transistor gate and an underlying semiconductor substrate,  
15      with such layer of silicon dioxide frequently being referred to as so-  
16      called "gate oxide". The thickness of the gate oxide can affect various  
17      electrical properties of a transistor structure incorporating the gate oxide,  
18      and accordingly it is desired to control the gate oxide thickness during  
19      device fabrication.

20      Transistor devices which are commonly used in semiconductor  
21      assemblies are PMOS transistor devices and NMOS transistor devices.  
22      Each type of transistor device has particular electrical properties  
23      associated therewith, and accordingly there can be advantages in utilizing

different gate oxide structures for some of the transistor devices associated with a semiconductor structure relative to others of the transistor devices associated with a semiconductor structure.

In light of the importance of gate oxide structures in semiconductor device fabrication, it is desired to develop new methods for forming oxide regions associated with semiconductor structures.

### SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming an oxide region over a semiconductor substrate. A nitrogen-containing layer is formed across at least some of the substrate. After the nitrogen-containing layer is formed, an oxide region is grown from at least some of the substrate. The nitrogen of the nitrogen-containing layer is dispersed within the oxide region.

In another aspect, the invention encompasses a method of forming a pair of transistors associated with a semiconductor substrate. A substrate is provided. A first region of the substrate is defined, and additionally a second region of the substrate is defined. The first region is a p-type doped region, and the second region is an n-type doped region. A first oxide region is formed which covers at least some of the first region of the substrate, and which does not cover any of the second region of the substrate. A nitrogen-comprising layer is formed across at least some of the first oxide region and across at least some of the

second region of the substrate. After the nitrogen-comprising layer is formed, a second oxide region is grown from the second region of the substrate. A first transistor gate is formed over the first oxide region, and a second transistor gate is formed over the second oxide region. First source/drain regions are formed proximate the first transistor gate to form a PMOS transistor comprising the first transistor gate. Second source/drain regions are formed proximate the second transistor gate to form an NMOS transistor comprising the second transistor gate.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional view of fragments of a semiconductor wafer shown at a preliminary processing step of the present invention.

Fig. 2 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 4.

1           Fig. 6 is a view of the Fig. 1 wafer fragments shown at a  
2 processing step subsequent to that of Fig. 5.

3           Fig. 7 is a diagrammatic, schematic, cross-sectional view of an  
4 exemplary remote plasma nitridation apparatus which can be utilized in  
5 methodology of the present invention.

6           Fig. 8 is a diagrammatic, cross-sectional view of another apparatus  
7 which can be utilized in methodology of the present invention.

8  
9           **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

10           This disclosure of the invention is submitted in furtherance of the  
11 constitutional purposes of the U.S. Patent Laws "to promote the progress  
12 of science and useful arts" (Article 1, Section 8).

13           A semiconductor wafer 10 is shown in fragmentary view in Fig. 1,  
14 and specifically is shown to comprise a first fragmentary region 12 and  
15 a second fragmentary region 14. Wafer 10 comprises a substrate 16.  
16 Substrate 16 can, for example, comprise a bulk semiconductive material,  
17 such as, for example, monocrystalline silicon lightly doped with a  
18 background p-type dopant. To aid in interpretation of the claims that  
19 follow, the terms "semiconductive substrate" and "semiconductor  
20 substrate" are defined to mean any construction comprising  
21 semiconductive material, including, but not limited to, bulk  
22 semiconductive materials such as a semiconductive wafer (either alone or  
23 in assemblies comprising other materials thereon), and semiconductive

1 material layers (either alone or in assemblies comprising other materials).  
2 The term "substrate" refers to any supporting structure, including, but  
3 not limited to, the semiconductive substrates described above.

4 Regions 12 and 14 can correspond to differently-doped regions of  
5 substrate 16. For instance, region 12 can correspond to a portion of  
6 substrate 16 having a heavier concentration of n-type conductivity  
7 enhancing dopant than p-type conductivity enhancing dopant, and can  
8 accordingly be referred to as an n-type doped region. Further, region  
9 14 can correspond to a region of substrate 16 wherein the p-type dopant  
10 concentration is heavier than any n-type dopant concentration, and can  
11 accordingly be referred to as a p-type region of substrate 10. In order  
12 to emphasize this aspect of the invention and assist in the description  
13 that follows, substrate 16 of region 12 is labeled with an "n", and region  
14 14 is labeled with a "p". It is to be understood that the shown doping  
15 of regions 12 and 14 corresponds to a particular embodiment of the  
16 present invention, and that other embodiments are encompassed wherein  
17 both of regions 12 and 14 are similarly doped, including embodiments  
18 wherein regions 12 and 14 are both heavier doped with n-type dopant  
19 than p-type dopant, as well as embodiments wherein regions 12 and 14  
20 are both heavier doped with p-type dopant than n-type dopant.

21 In particular embodiments of the present invention, regions 12 and  
22 14 correspond to portions of a semiconductor memory assembly, and in  
23 such embodiments regions 12 and 14 can both correspond to memory

array regions, or can both correspond to regions peripheral to a memory array region, or alternatively one of regions 12 and 14 can correspond to a memory array region while the other regions 12 and 14 corresponds to a portion of the wafer peripheral to the memory array region.

Referring to Fig. 2, an oxide layer 18 is formed over substrate 16. Oxide 18 is shown formed over both of regions 12 and 14. Oxide layer 18 can comprise, for example, silicon dioxide, and can be formed by, for example, chemical vapor deposition over substrate 16. Alternatively, oxide layer 18 can be formed by exposing substrate 16 to oxidizing conditions. For instance, if substrate 16 comprises monocrystalline silicon, a silicon dioxide layer 18 can be formed by oxidizing a surface of substrate 16. Oxide layer 18 is preferably formed to a thickness of less than 70Å, and can be formed to a thickness of less than or equal to about 50Å, such as, for example, a thickness of about 30Å.

A patterned masking layer 20 is shown formed over oxide layer 18 to mask the portion of oxide layer 18 in region 12, while leaving the portion of oxide layer 18 of region 14 exposed. Masking layer 20 can comprise, for example, photoresist, and can be patterned by photolithographic processing. Although masking layer 20 is shown covering an entirety of oxide 18 of region 12, and not covering any of oxide 18 of region 14, it is to be understood that the invention encompasses other embodiments wherein masking layer 20 covers only a



1 portion of oxide 18 over region 12, and further encompasses  
2 embodiments wherein masking layer 20 also covers a portion of oxide  
3 layer 18 of region 14.

4 Referring to Fig. 3, the exposed portion of oxide 18 of region 14  
5 is removed. Such can be accomplished by, for example, exposing  
6 wafer 10 to hydrofluoric acid. Masking layer 20 (Fig. 2) protects  
7 oxide 18 from being exposed to the oxide-removing etchant, and  
8 accordingly oxide 18 remains over region 12 after removal of oxide 18  
9 from region 14.

10 It is to be understood that the processing of Figs. 2 and 3 is but  
11 one exemplary method of forming the structure shown in Fig. 3, and  
12 that other methods are encompassed by the present invention. In any  
13 event, the structure corresponding to Fig. 3 is preferably ultimately  
14 formed, with such structure having oxide 18 covering at least some of  
15 region 12 of substrate 16, and not covering at least some of region 14  
16 of substrate 16.

17 Referring to Fig. 4, a nitrogen-comprising layer 22 is formed over  
18 regions 12 and 14. More specifically, nitrogen-comprising layer 22 is  
19 formed on and/or within at least some of oxide layer 18 of region 12,  
20 and further is formed on and/or within at least some of substrate 16 of  
21 region 14. Nitrogen-comprising layer 22 is preferably kept within a  
22 surface region of oxide 18 of region 12, and also within a surface region  
23 of substrate 16 of region 14. For purposes of interpreting this disclosure

1 and the claims that follow, a surface region is defined to be a region  
2 which extends to no more than 10Å beneath a surface, and in particular  
3 embodiments nitrogen-comprising region 22 extends no more than 5Å  
4 beneath an upper surface of either substrate 16 of region 14 or oxide 18  
5 of region 12.

6 Nitrogen-comprising region 22 can be formed by, for example,  
7 remote plasma nitridization utilizing, for example, an apparatus 200  
8 described with reference to Fig. 7. Apparatus 200 comprises a plasma  
9 chamber 202 and a reaction chamber 204. Reaction chamber 204  
10 comprises a substrate holder 206, and substrate 16 is supported within  
11 chamber 204 by holder 206. Preferably, holder 206 is configured to  
12 rotate substrate 16 during exposure of substrate 16 to activated nitrogen  
13 species. Such activated nitrogen species are formed within plasma  
14 chamber 202 by, for example, exposing N<sub>2</sub> and/or other nitrogen-  
15 containing materials (for example, N<sub>2</sub>O and/or NH<sub>3</sub>) to plasma conditions,  
16 with the term "activated" indicating that the nitrogen species is different  
17 than the form of nitrogen fed to the plasma. An activated nitrogen  
18 species can comprise, for example, a nitrogen ion or a nitrogen atom in  
19 an energy state higher than its ground state. Exemplary plasma  
20 conditions comprise utilization of a microwave plasma generator at a  
21 power of from about 1,500 watts to about 3,000 watts, and a pressure  
22 within chamber 202 of less than or equal to about 3 Torr.  
23

1           The plasma of chamber 202 forms activated nitrogen species which  
2 migrate along a passageway 208 into chamber 204 whereupon the species  
3 can form nitrogen-comprising layer 22 (Fig. 4) over substrate 16. An  
4 arrow is shown within passageway 208 to indicate migration of plasma  
5 activated nitrogen species through passageway 208.

6           Preferably, passageway 208 is of sufficient length so that  
7 plasma 202 is at least about 12 inches from substrate 16. Such can  
8 enable highly activated nitrogen species formed within a plasma to relax  
9 prior to interaction with substrate 16, which can limit penetration of the  
10 nitrogen species into substrate 16 relative to an amount of penetration  
11 which would occur with more highly activated species. In order to  
12 further limit penetration of nitrogen species into substrate 16,  
13 substrate 16 is preferably not biased relative to the plasma within  
14 chamber 202.

15           Suitable operating conditions for forming a nitrogen-comprising  
16 plasma over substrate 16 can include maintaining a temperature of  
17 substrate 16 at from about 550°C to about 1,000°C, rotating the wafer  
18 at about 90 rotations per minute (RPM), maintaining a pressure within  
19 chambers 202 and 204 of from about 0.8 Torr to about 2.8 Torr, and  
20 exposing the wafer to the nitridization conditions for a time of from  
21 about one minute to about five minutes.

22           An alternative apparatus which can be utilized for forming  
23 nitrogen-comprising layer 22 (Fig. 4) is described with reference to Fig. 8

as apparatus 220. Apparatus 220 can be referred to as a high density plasma remote plasma nitridization (HDP-RPN) apparatus, or simply as a plasma nitridization (PN) apparatus. Apparatus 220 comprises a reaction chamber 222 having a wafer holder 224 therein. Wafer 16 is supported on holder 224. A plasma 226 is formed above substrate 16, and preferably is maintained a distance "X" from substrate 16, with distance "X" corresponding to at least about four inches. Nitrogen is introduced into plasma 226 in the form of, for example, N<sub>2</sub>, and activated nitrogen species are formed from the nitrogen. Suitable processing parameters for utilization of the apparatus of Fig. 8 include a wafer temperature of from 0°C to 400°C, no rotation of the wafer, a pressure within chamber 222 of from about 5 mTorr to about 15 mTorr (preferably of from about 5 mTorr to about 10 mTorr), and an exposure time of substrate 16 to activated nitrogen species within chamber 222 of from about 5 seconds to about 30 seconds.

Referring next to Fig. 5, substrate 10 is shown at a processing step subsequent to that of Fig. 4, and specifically is shown after exposure to oxidizing conditions. The oxidizing conditions grow an oxide layer 24 from region 14 of substrate 16. The portion of nitrogen-comprising layer 22 previously over region 14 (Fig. 4) is dispersed within oxide 24, and preferably becomes sufficiently dispersed so that the nitrogen does not significantly affect performance characteristics of the oxide in devices incorporating the oxide. Suitable processing forms oxide layer 24 to be

1 at least about 70Å thick. Such processing is found to adequately  
2 distribute nitrogen of the previous layer 22 that had been associated with  
3 region 14 so that oxide layer 24 can be incorporated as a gate oxide in  
4 transistor devices.

5 It is noted that nitrogen-comprising layer 22 over oxide 18 of  
6 region 12 substantially slows further oxidation of substrate 16 within  
7 region 12, and accordingly oxide grows faster over region 14 than over  
8 region 12. Thus, oxide 24 is formed to be thicker than the oxide 18  
9 over region 12. Further, nitrogen-comprising layer 22 associated with  
10 region 12 remains substantially intact and it can be utilized as, for  
11 example, a dopant barrier layer for devices subsequently formed over  
12 region 12. In particular aspects of the present invention, the oxidation  
13 of wafer 10 forms oxide layer 24 to be at least about 70Å thick, and  
14 oxide layer 18 remains less than or equal to about 50Å thick.

15 Referring to Fig. 6, transistor devices 30 and 32 are formed to be  
16 associated with regions 12 and 14, respectively. Devices 30 and 32  
17 comprise oxide layers 18 and 24 as gate oxide, respectively. Device 30  
18 further comprises layers 34, 36 and 38 patterned over oxide 18, and  
19 device 32 further comprises layers 40, 42 and 44 patterned over oxide  
20 layer 24.

21 Referring to device 30, layers 34 and 36 can comprise, for  
22 example, conductive materials such as, for example, conductively doped  
23 silicon and metal silicide, respectively; and layer 38 can comprise, for

example, an insulative cap, such as, for example, a silicon nitride cap. Transistor device 30 can comprise a PMOS device, and conductively doped silicon layer 34 can comprise p-type doped polysilicon. Nitrogen-comprising layer 22 can function as a barrier layer to impede migration of p-type dopant from layer 34 into substrate 16. It is noted that the portion of substrate 16 under oxide layer 18 is an n-type channel for PMOS device 30. Accordingly, if p-type dopant migrates from layer 34 into substrate 16, it can alter dopant concentrations within the n-type channel, and affect or destroy operation of device 30.

Referring to device 32, layers 40, 42 and 44 can comprise, for example, conductively doped silicon, metal silicide, and an insulative cap, respectively. Conductively doped silicon 40 can comprise, for example, n-type doped polysilicon, and metal silicide 42 can comprise, for example, titanium silicide or tungsten silicide. Insulative cap 44 can comprise, for example, a silicon nitride cap. Device 32 corresponds to an NMOS transistor device.

Conductive layers 40 and 42 form a gate for device 32, and conductive layers 34 and 36 form a gate for device 30. Sidewall spacers 46 are shown formed along sidewalls of the gates of devices 30 and 32. Layers 34, 36, 38, 40, 42 and 44, as well as sidewall spacers 46, can be formed by conventional methods.

Lightly doped diffusion regions 48 are shown formed within substrate 16 and proximate a channel region of device 32, and heavily

1 doped source/drain regions 50 are also shown formed within substrate 16  
2 and associated with device 32. The gate defined by conductive  
3 materials 40 and 42 gatedly connects the source/drain regions 50 with  
4 one another. Source/drain regions 50 and LDD regions 48 can be  
5 formed by conventional methods, and source/drain regions 50 can be  
6 heavily doped with n-type conductivity enhancing dopant as is typical for  
7 an NMOS device 32.

8 Lightly doped diffusion regions 52 are shown formed within  
9 region 12 of substrate 16 and heavily doped source/drain regions 54 are  
10 also shown within region 12 of substrate 16, and shown associated with  
11 device 30. A transistor gate defined by conductive layers 34 and 36  
12 gatedly connects source/drain regions 54 with one another. Source/drain  
13 regions 54 can be heavily doped with p-type dopant as is typical for a  
14 PMOS transistor device 30.

15 Lightly doped diffusion regions 48 and 52 would typically be lightly  
16 doped with n-type conductivity enhancing dopant and p-type conductivity  
17 enhancing dopant, respectively. The term "lightly doped" is used to  
18 indicate that the diffusion regions 48 and 52 are more lightly doped than  
19 are source/drain regions 50 and 54. Typically, source/drain regions 50  
20 and 54 would be doped to a concentration of at least about  
21  $10^{19}$  atoms/cm<sup>3</sup> with conductivity enhancing dopant.

22 In compliance with the statute, the invention has been described  
23 in language more or less specific as to structural and methodical

1 features. It is to be understood, however, that the invention is not  
2 limited to the specific features shown and described, since the means  
3 herein disclosed comprise preferred forms of putting the invention into  
4 effect. The invention is, therefore, claimed in any of its forms or  
5 modifications within the proper scope of the appended claims  
6 appropriately interpreted in accordance with the doctrine of equivalents.



1        **CLAIMS:**

2            1.     A method of forming an oxide region over a semiconductor  
3 substrate, comprising:

4            forming a nitrogen-containing layer across at least some of the  
5 substrate; and

6            after forming the nitrogen-containing layer, growing an oxide region  
7 from the at least some of the substrate, the nitrogen of the nitrogen-  
8 containing layer being dispersed within the oxide region.

9  
10           2.     The method of claim 1 wherein the substrate comprises  
11 silicon and the oxide region comprises silicon dioxide.

12  
13           3.     The method of claim 1 wherein the substrate comprises  
14 monocrystalline silicon and the oxide region is grown from the  
15 monocrystalline silicon and comprises silicon dioxide.

16  
17           4.     The method of claim 1 wherein the nitrogen-comprising layer  
18 is formed from plasma activated nitrogen species.

1           5.     The method of claim 1 wherein the nitrogen-comprising layer  
2 is formed by remote plasma nitridation utilizing nitrogen species  
3 generated in a plasma that is at least about 12 inches from the  
4 substrate.

5  
6           6.     The method of claim 1 wherein the nitrogen-comprising layer  
7 is formed by remote plasma nitridation utilizing nitrogen species  
8 generated in a plasma that is at least about 12 inches from the  
9 substrate; and wherein the substrate not being biased relative to the  
10 plasma during formation of the nitrogen-comprising layer.

11  
12           7.     The method of claim 6 wherein the substrate is maintained  
13 at a temperature of from about 550°C to about 1000°C during formation  
14 of the nitrogen-comprising layer.

15  
16           8.     The method of claim 6 wherein the substrate is exposed to  
17 the nitrogen species for a time of from greater than 0 minutes to about  
18 about 5 minutes.

19  
20           9.     The method of claim 1 wherein the nitrogen-comprising layer  
21 is formed by plasma nitridation utilizing nitrogen species generated in a  
22 plasma that is at least about 4 inches from the substrate.  
23

1           10. The method of claim 9 wherein the substrate is maintained  
2 at a temperature of from about 0°C to about 400°C during formation  
3 of the nitrogen-comprising layer.  
4

5           11. The method of claim 9 wherein the substrate is exposed to  
6 the nitrogen species for a time of from greater than 0 seconds to about  
7 about 30 seconds.  
8

9           12. A method of forming a pair of oxide regions over a  
10 semiconductor substrate, comprising:

11           forming a first oxide region which covers only a portion of the  
12 substrate;

13           forming a nitrogen-comprising layer across at least some of the  
14 first oxide region and across at least some of the substrate that is not  
15 covered by the first oxide region; and

16           after forming the nitrogen-comprising layer, growing a second oxide  
17 region from the at least some of the substrate.  
18  
19  
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13. The method of claim 12 wherein the first oxide region is formed by:

forming an oxide layer over the covered region and at least some of the uncovered region of the substrate; and  
removing the oxide layer from over the uncovered region of the substrate.

14. The method of claim 13 wherein the oxide layer is formed by exposing the substrate to oxidizing conditions.

15. The method of claim 12 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

16. The method of claim 12 wherein the nitrogen-comprising layer is formed by plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

17. A method of forming a pair of transistors associated with a semiconductor substrate, comprising:

defining a first region and a second region of the substrate;

forming a first oxide region which covers at least some of the first region of the substrate and which does not cover at least some of the second region of the substrate;

forming a nitrogen-comprising layer across at least some of the first oxide region and across at least some of the uncovered second region of the substrate;

after forming the nitrogen-comprising layer, growing a second oxide region from the uncovered second region of the substrate;

forming a first transistor gate over the first oxide region and a second transistor gate over the second oxide region;

forming first source/drain regions proximate the first transistor gate; and

forming second source/drain regions proximate the second transistor gate.

18. The method of claim 17 wherein the second oxide region is grown to be thicker than the first oxide region.

1           19. The method of claim 17 wherein the first oxide region is  
2 formed by:

3           forming an oxide layer over the first and second regions of the  
4 substrate; and

5           removing the oxide layer from over the at least some of the  
6 second region of the substrate.

7  
8           20. The method of claim 17 wherein the substrate comprises  
9 silicon and the oxide regions comprise silicon dioxide.

10  
11           21. The method of claim 17 wherein the substrate comprises  
12 monocrystalline silicon and the oxide regions comprise silicon dioxide;  
13 and wherein the first oxide region is grown from the monocrystalline  
14 silicon substrate.

15  
16           22. The method of claim 17 wherein the nitrogen-comprising  
17 layer is formed by remote plasma nitridation utilizing nitrogen species  
18 generated in a plasma that is at least about 12 inches from the  
19 substrate.

1           23. The method of claim 17 wherein the nitrogen-comprising  
2 layer is formed by plasma nitridation utilizing nitrogen species generated  
3 in a plasma that is at least about 4 inches from the substrate.  
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23

1           24. A method of forming a pair of transistors associated with a  
2 semiconductor substrate, comprising:

3           defining a first region and a second region of the substrate, the  
4 first region being a p-type doped region and the second region being an  
5 n-type doped region;

6           forming a first oxide region which covers at least some of the first  
7 region of the substrate and which does not cover any of the second  
8 region of the substrate;

9           forming a nitrogen-comprising layer across at least some of the  
10 first oxide region and across at least some of the second region of the  
11 substrate;

12          after forming the nitrogen-comprising layer, growing a second oxide  
13 region from the second region of the substrate;

14          forming a first transistor gate over the first oxide region and a  
15 second transistor gate over the second oxide region;

16          forming first source/drain regions proximate the first transistor gate  
17 to form a PMOS transistor comprising the first transistor gate; and

18          forming second source/drain regions proximate the second transistor  
19 gate to form an NMOS transistor comprising the second transistor gate.  
20  
21  
22  
23



1           25.    The method of claim 24 wherein the PMOS transistor gate  
2 comprises p-type doped silicon, and wherein the nitrogen-containing layer  
3 formed over the oxide region prevents p-type dopant migration from the  
4 doped silicon to the first substrate region.

5  
6           26.    The method of claim 24 wherein the second oxide region is  
7 grown to be thicker than the first oxide region.

8  
9           27.    The method of claim 24 wherein the nitrogen-comprising  
10 layer is formed by remote plasma nitridation utilizing nitrogen species  
11 generated in a plasma that is at least about 12 inches from the  
12 substrate.

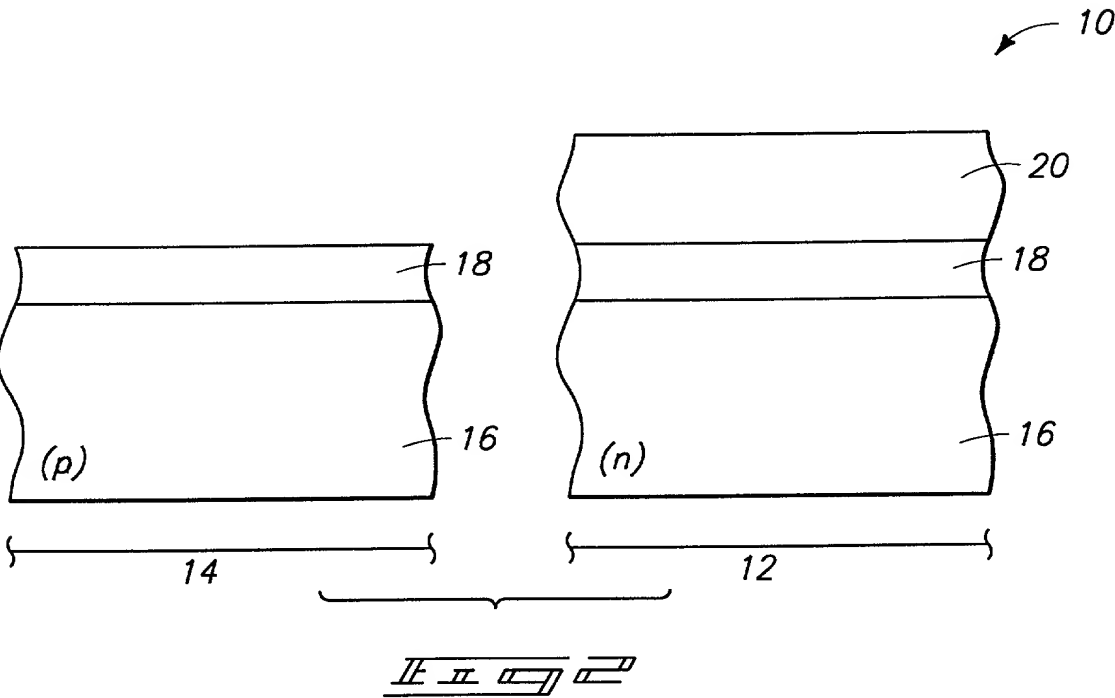
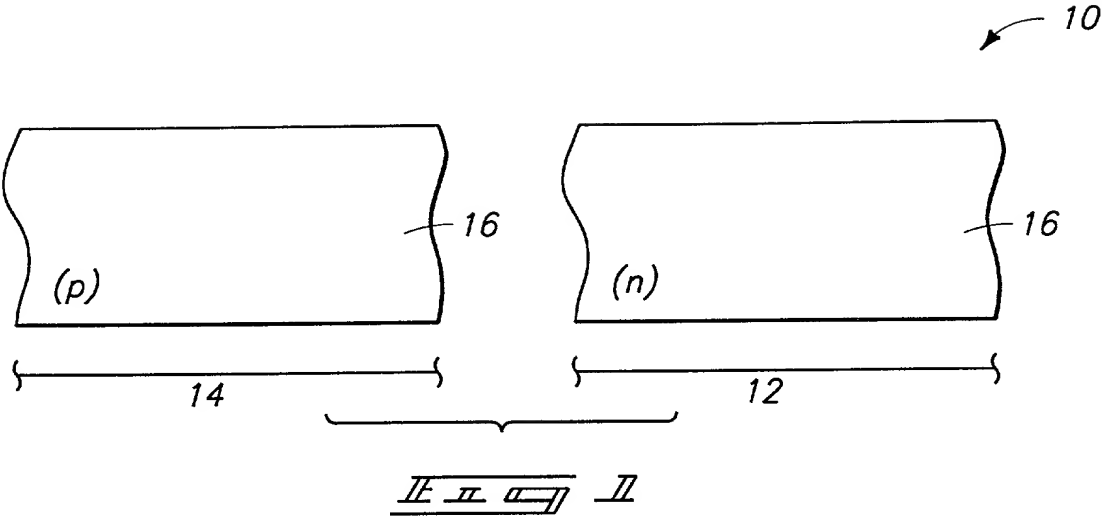
13  
14           28.    The method of claim 24 wherein the nitrogen-comprising  
15 layer is formed by plasma nitridation utilizing nitrogen species generated  
16 in a plasma that is at least about 4 inches from the substrate.

1     ABSTRACT OF THE DISCLOSURE

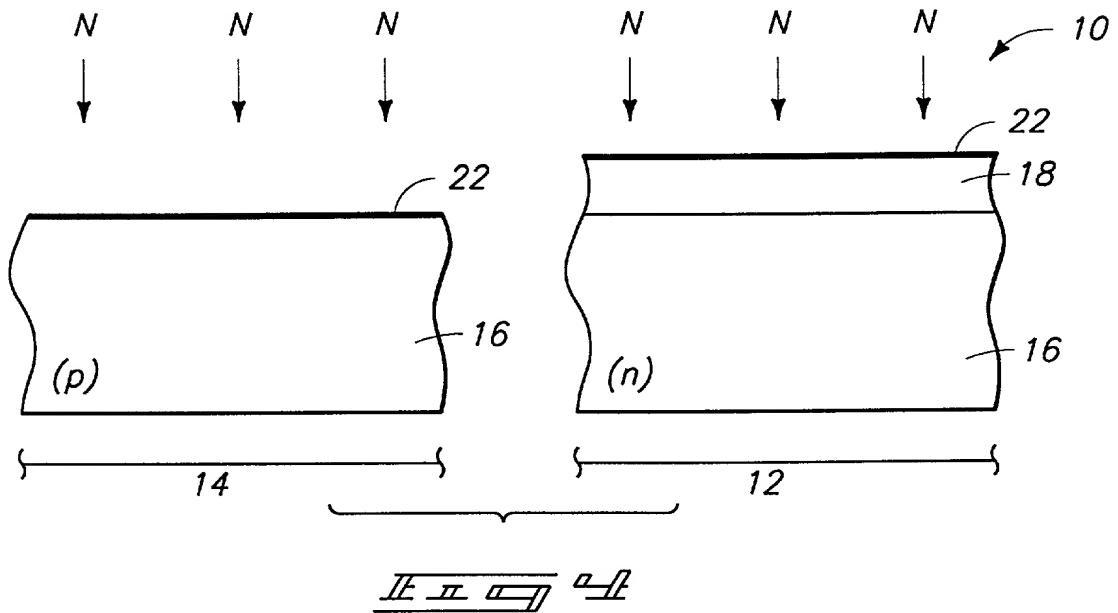
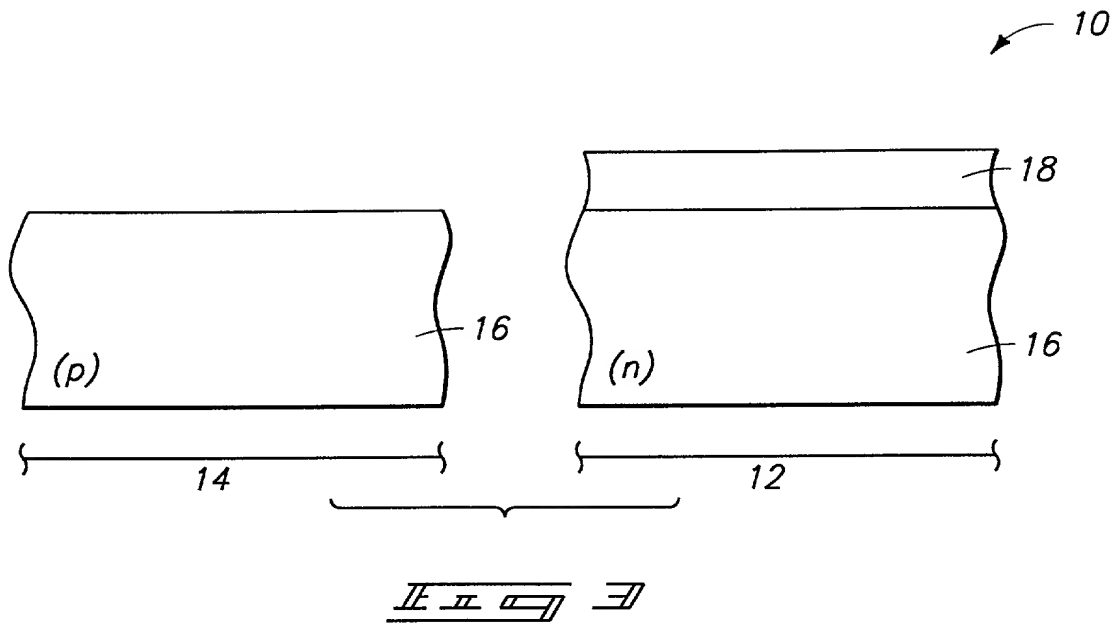
2             The invention encompasses a method of forming an oxide region  
3 over a semiconductor substrate. A nitrogen-containing layer is formed  
4 across at least some of the substrate. After the nitrogen-containing layer  
5 is formed, an oxide region is grown from at least some of the substrate.  
6 The nitrogen of the nitrogen-containing layer is dispersed within the  
7 oxide region. The invention also encompasses a method of forming a  
8 pair of transistors associated with a semiconductor substrate. A substrate  
9 is provided. A first region of the substrate is defined, and additionally  
10 a second region of the substrate is defined. A first oxide region is  
11 formed which covers at least some of the first region of the substrate,  
12 and which does not cover any of the second region of the substrate.  
13 A nitrogen-comprising layer is formed across at least some of the first  
14 oxide region and across at least some of the second region of the  
15 substrate. After the nitrogen-comprising layer is formed, a second oxide  
16 region is grown from the second region of the substrate. A first  
17 transistor gate is formed over the first oxide region, and a second  
18 transistor gate is formed over the second oxide region.

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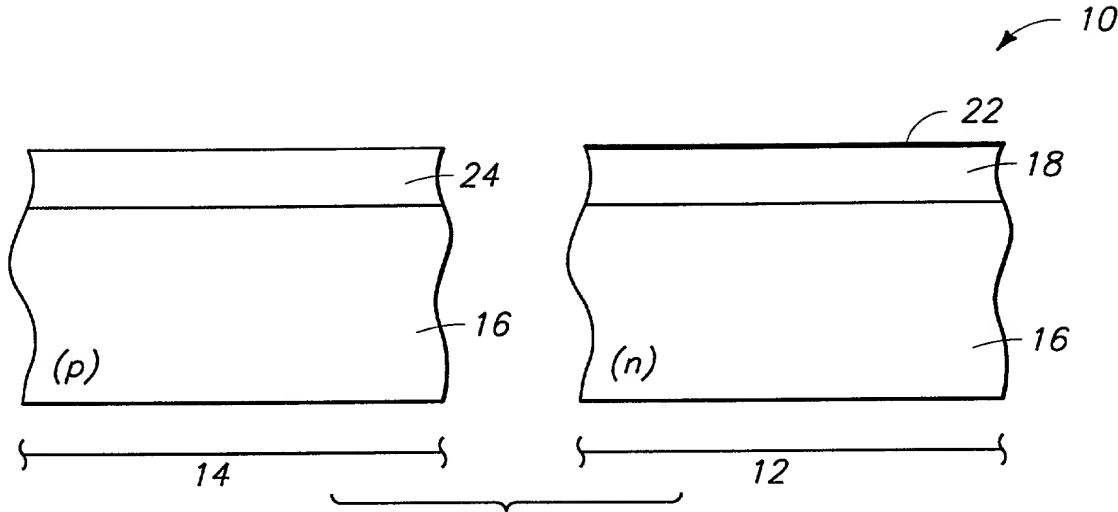


Fig. 5

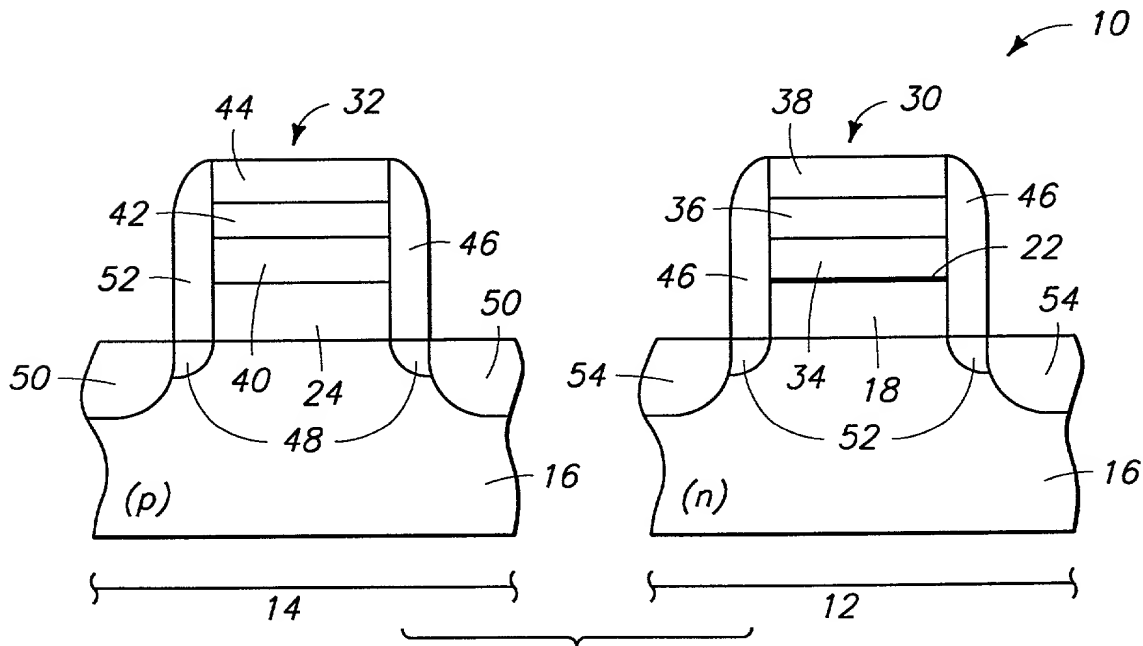
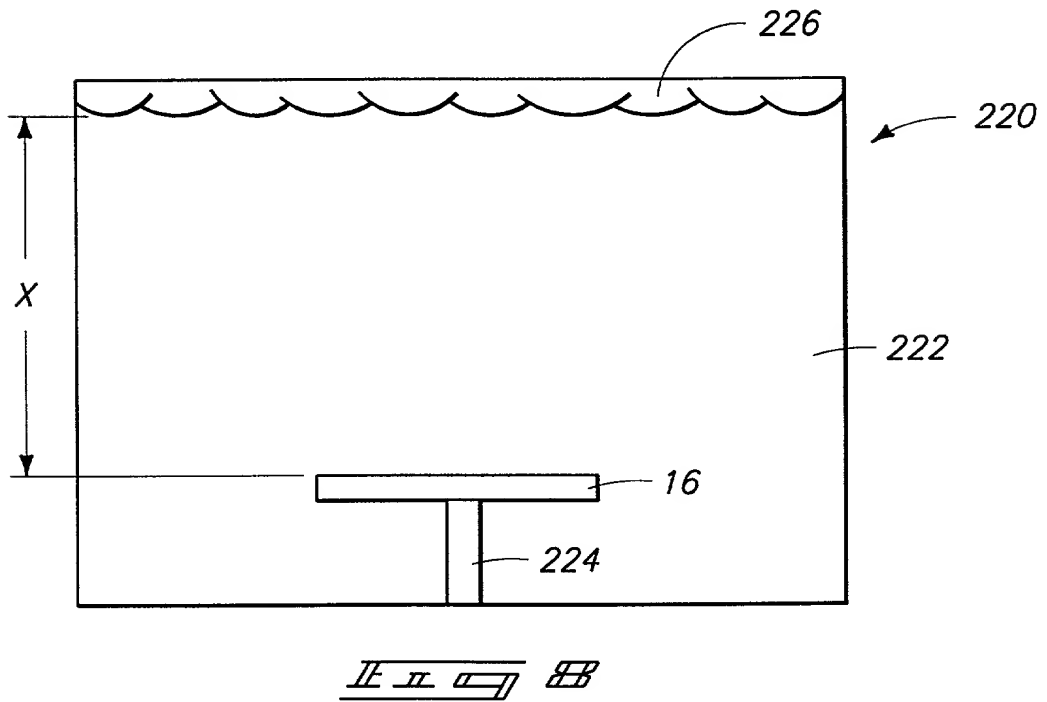
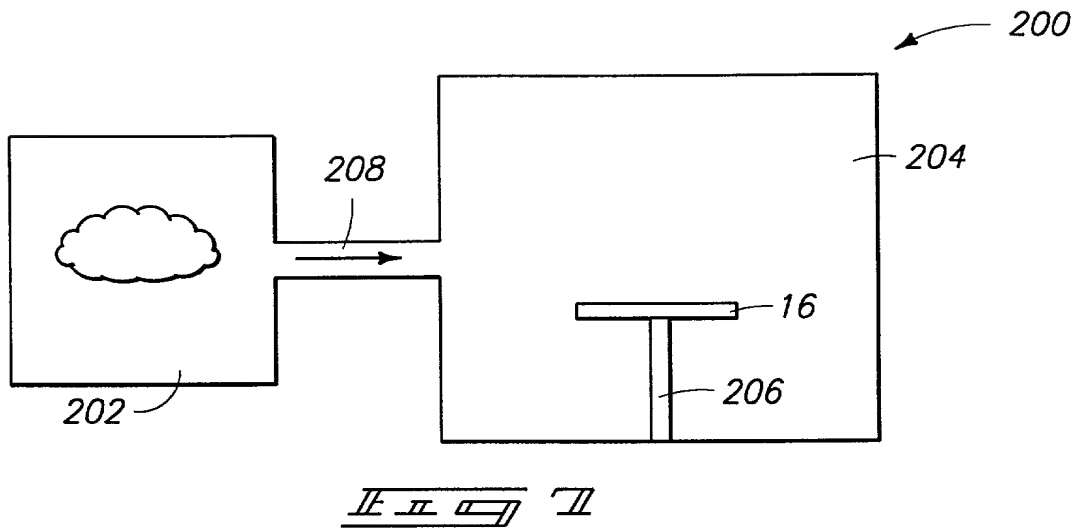


Fig. 6

4/4



**DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION**

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming Oxide Regions Over Semiconductor Substrates, and Methods of Forming Transistors Associated With Semiconductor Substrates, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

**PRIOR FOREIGN APPLICATIONS:**

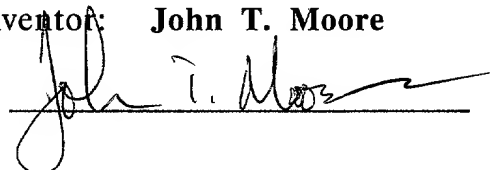
I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were

1 made with the knowledge that willful false statements and the like so  
2 made are punishable by fine or imprisonment, or both, under  
3 Section 1001 of Title 18 of the United States Code and that such willful  
4 false statement may jeopardize the validity of the application or any  
5 patent issued therefrom.

6  
7 \* \* \* \* \*

8  
9 Full name of sole inventor: **John T. Moore**

10 Inventor's Signature: 

11 Date: 6/14/00

12 Residence: **Boise, ID**

13 Citizenship: **US**

14 Post Office Address: **12530 W. Lexus Ct.**  
**Boise, ID 83713**



1                   **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2   Application Serial No. .... Filed herewith  
 3   Filing Date ..... Filed herewith  
 4   Inventor ..... John T. Moore  
 5   Assignee ..... Micron Technology, Inc  
 6   Group Art Unit ..... Unknown  
 7   Examiner ..... Unknown  
 8   Attorney's Docket No. .... MI22-1384  
 9   Title: Methods of Forming Oxide Regions Over Semiconductor Substrates, and  
 10       Methods of Forming Transistors Associated With Semiconductor Substrates

11                   **POWER OF ATTORNEY BY ASSIGNEE AND**  
 12                   **CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)**

13   To:   Assistant Commissioner for Patents  
 14       Washington, D.C. 20231

15   Sir:

16                   **MICRON TECHNOLOGY, INC.**, the Assignee of the entire right,  
 17   title and interest in the above-identified patent application by assignment  
 18   attached hereto, hereby appoints the attorneys and agents of the firm of  
 19   **WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S.**, listed as  
 20   follows:

21   David P. Roberts	Reg. No. 23,032
22   Randy A. Gregory	Reg. No. 30,386
23   Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
George G. Grigel	Reg. No. 31,166
Keith D. Grzelak	Reg. No. 37,144
James D. Shaurette	Reg. No. 39,833
Frederick M. Fliegel	Reg. No. 36,138
Donald Brent Kenady	Reg. No. 40,045

James E. Lake  
Bernard Berman

Reg. No. 44,854  
Reg. No. 37,279

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas  
Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys  
with full power of substitution to prosecute this application and transact  
all business in the Patent and Trademark Office connected therewith.

The Assignee certifies that the above-identified Assignment has  
been reviewed and to the best of Assignee's knowledge and belief, title  
is in the Assignee, and a copy of the Assignment is submitted herewith.

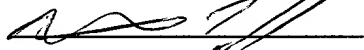
Please direct all correspondence regarding this application to:

Customer No. 021567  
Wells, St. John, Roberts, Gregory & Matkin P.S.  
Attn: David G. Latwesen, Ph.D.  
601 W. First Avenue, Suite 1300  
Spokane, WA 99201-3828

Telephone: (509) 624-4276  
Facsimile: (509) 838-3424

MICRON TECHNOLOGY, INC.

Dated: 6-16-00

By: 

Name: Michael L. Lynch, Esq.  
Title: Chief Patent Counsel

*Attachment: Copy of Assignment; Copy of Board of Directors' Resolution*

[illegible]

**NOW THEREFORE BE IT RESOLVED**, that the Board hereby approves and authorizes Mr. Michael L. Lynch, Assistant General Counsel for Intellectual Property, to execute on behalf of the Company, documents pertaining to the Company's patent prosecution matters, including but not limited to documents relating to representation before a patent examining authority, patent terms and other patent prosecution procedures, both in the United States and other countries, upon such terms and conditions as the General Counsel of the Company shall deem necessary or appropriate.

**MICRON TECHNOLOGY, INC.  
CERTIFIED COPY OF RESOLUTIONS**

I, Jan R. Reimer, the Assistant Secretary of Micron Technology, Inc. do hereby certify, that the resolutions attached hereto represent a complete, true and correct copy of the resolutions duly adopted by the Board of Directors of Micron Technology, Inc., a corporation duly organized and existing under the laws of the State of Delaware, at a meeting duly held on March 25, 1996, a quorum being present, and have been entered into the minutes of said meeting; that I am the keeper of the corporate seal and of the minutes and records of this Corporation; and that the said resolutions have not been rescinded or modified.

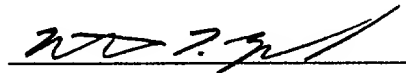
The resolutions attached hereto are in conformity with the Articles of Incorporation and Bylaws of the Corporation and are now in full force and effect.

I further certify that the person whose name and signature is set out below is the person authorized to act for said corporation in transactions with and pursuant to the foregoing resolutions, and that such person is now duly qualified and acting in his respective capacity:

NAME AND TITLE

SIGNATURE

Michael L. Lynch, Assistant General  
Counsel for Intellectual Property



IN WITNESS WHEREOF, I have hereunto subscribed my name and affixed the seal of the said corporation, this 16th day of May, 1996.

  
Jan R. Reimer, Assistant Secretary

(SEAL)

002290-9620960